16(Amended). A functional circuit comprising: an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information packets put onto the interconnect by one or more modules, said monitoring circuit comprising:

circuitry for determining if the information packet on the interconnect matches one or more conditions; and

circuitry for preventing a module from putting further information onto said interconnect if it is determined that information packet on the interconnect matches said one or more conditions.

17(Amended). A circuit as claimed in claim 16, wherein the functional circuit is an integrated circuit.

24(Amended). A circuit comprising:

an interconnect;

one or more modules connected to the interconnect to put information packets onto the interconnect;

an arbiter for determining which module is permitted to put information packets onto the interconnect; and

circuitry for preventing a module from putting further information packets onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25(Amended). A method comprising the steps of:

monitoring information packets on an interconnect, the information being put onto the interconnect by one or modules; determining if the information on an interconnect satisfies one or more conditions; and

preventing a module from putting information packets onto an interconnect if it is determined that the information satisfies one or more conditions.

REMARKS/ARGUMENTS

Claims 1-25 remain in this application. Claim 1 is amended to incorporate the limitations of claim 2, and claim 2 is cancelled. Claim 16-17 are amended to correct an informality in the claims as filed. Claims 24-25 are amended to more distinctly

describe the invention. No new matter is added by these amendments and the amendments are not intended to affect the scope of the claims.

A. Rejections under 35 U.S.C. 112

Claims 17-23 were rejected under 35 U.S.C. 112. This rejection is respectfully traversed. Claim 16 is amended to clarify the distinction between the two circuits that appeared in the claim as filed. Corresponding amendments are made to claims 17-23. These amendments are believed to overcome the rejection to claims 16-23.

B. Double patenting

A suitable terminal disclaimer will be supplied upon indication of allowable subject matter.

C. Rejections under 35 U.S.C. 102

Claims 1, 3, 7-9, 11-14, 16 and 18-25 were rejected under 35 U.S.C. 102 as anticipated by Wolff et al. This rejection is respectfully traversed.

Independent claims 1, 16 and 25 call for, in varying language, monitoring packet information on an interconnect. At least this feature of the independent claims is not shown or suggested in the Wolff et al. reference. Wolff et al. does not show or suggest using a packet interconnect. Wolff et al. contemplate monitoring the signals that pass on an interconnect (see column 4, lines 64-68), but not packets. A common definition of a packet in a data communication network is: "A group of bits, including data and control elements that is switched and transmitted as a unit" (Modern Dictionary of Electronics, Sixth Ed., Howard W. Sams & Company, 1988). Nothing in Wolff et al. would suggest this packet feature of the instant claims.

Moreover, Wolff et al. do not monitor information from the interconnect as that term is used in the instant application. Wolff et al suggest monitoring the signals to detect error conditions, and suggest deriving parity information from the signals, but do not show or suggest directly monitoring the information itself. There is a significant difference between monitoring signals for an error condition, and

monitoring information contained within a packet as called for by independent claims 1, 16 and 25.

Dependent claims 3, 7-9, 11-14, and 18-23 are believed to be allowable for at least the same reasons as the claims from which they depend. In particular, the Office Action asserts that the "information comprising packets of information" is inherent is incorrect. Packet data transfer is substantially different from the bus data transfer mechanisms contemplated by Wolff, and if the examiner maintains this position supporting references are required. Further, the assertion in the Office Action that the cycle definition signal suggests the limitation of claim three plainly misconstrues the reference. A cycle definition signal has nothing to do with the information that is being carried, and everything to do with the clock signals used on the bus. This does not show or suggest this feature of claim 3.

For at least these reasons, claims 1, 3, 7-9, 11-14, 16 and 18-25 are believed to be allowable over Wolff et al.

D. Rejections under 35 U.S.C. 103

Claims 4-6 were rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Cepulis et al. This rejection is respectfully traversed. Claims 4-6 depend from claim 1 and are believed to distinguish over Wolff et al. for at least the same reasons as claim 1. Cepulis et al. do not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

Claim 10 was rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Ardini, Jr. et al. This rejection is respectfully traversed. Claim 10 depends from claim 1 and is believed to distinguish over Wolff et al. for at least the same reasons as claim 1. The Ardini reference does not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

Claims 15 was rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Pizzicia. This rejection is respectfully traversed. Claims 15 depends from claim 1 and is believed to distinguish over Wolff et al. for at least the same reasons as claim 1. Pizzicia does not supply the deficiencies noted above as, like Wolff et al.,

the reference does not contemplate packet interconnects.

Claims 17 were rejected under 35 U.S.C. 103 as unpatentable over Wolff et al. in view of Bershteyn et al. This rejection is respectfully traversed. Claims 17 depends from claim 16 and is believed to distinguish over Wolff et al. for at least the same reasons as claim 16. Bershteyn et al. do not supply the deficiencies noted above as, like Wolff et al., the reference does not contemplate packet interconnects.

E. Conclusion

In view of all of the above claims 1-25 are believed to be allowable and the case in condition for allowance which action is respectfully requested. The references that were cited and not relied upon are believed to be no more pertinent that those references that were relied upon.

No fee is believed to be required by this response as determined on the accompanying transmittal letter. Should any other fee be required, please charge Deposit 50-1123. Should any extension of time be required please consider this a petition therefore and charge the required fee to Deposit Account 50-1123. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made"**

Respectfully submitted,

Date: August 7, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

A. In the claims

1(Amended). A circuit for monitoring packet information put onto an interconnect by one or more modules, said circuit comprising:

circuitry for determining if the information [on the interconnect] in a packet matches one or more conditions; and

circuitry for preventing a module from putting further information packets onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.

2. Cancelled.

16(Amended). A functional circuit comprising: an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information packets put onto the interconnect by one or more modules, said monitoring circuit comprising:

circuitry for determining if the information packet on the interconnect matches one or more conditions; and

circuitry for preventing a module from putting further information onto said interconnect if it is determined that information packet on the interconnect matches said one or more conditions.

17(Amended). A circuit as claimed in claim 16, wherein the functional circuit is an integrated circuit.

24(Amended). A circuit comprising:

an interconnect;

one or more modules connected to the interconnect to put information packets onto the interconnect;

an arbiter for determining which module is permitted to put information packets onto the interconnect; and

circuitry for preventing a module from putting further information packets onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25(Amended). A method comprising the steps of:

monitoring information packets on an interconnect, the information being put onto the interconnect by one or modules; determining if the information on an interconnect satisfies one or more conditions; and

preventing a module from putting information packets onto an interconnect if it is determined that the information satisfies one or more conditions.